SP5502

1.3GHz I²C BUS 4-Address Synthesiser

Supersedes version in April 1994 Consumer IC Handbook, HB3120 - 2.0 DS3031 - 5.0 January 1997

The SP5502 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The SP5502 has four programmable I²C BUS addresses, which allows two or more synthesisers to be used in a system.

The device is available in two variants: the SP5502F in 14-lead miniature plastic package (MP14) and the SP5502S in 16-lead miniature plastic package (MP16). See Features below for functional differences between the devices.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (240mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 5×20mA Controllable Outputs (SP5502S)
- 3×20mA Controllable Outputs (SP5502F)
- Variable I²C BUS Address for Multi-Tuner Applications
- ESD Protection *

* Normal ESD handling precautions should be observed.

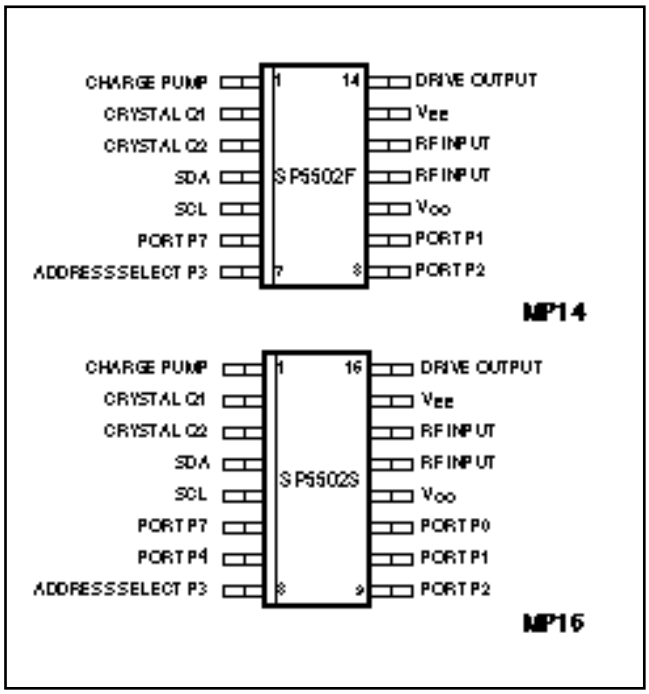


Fig. 1 Pin connections – top view

APPLICATIONS

- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5502F KG MPAS (14-lead miniature plastic package)
SP5502S KG MPAS (16-lead miniature plastic package)

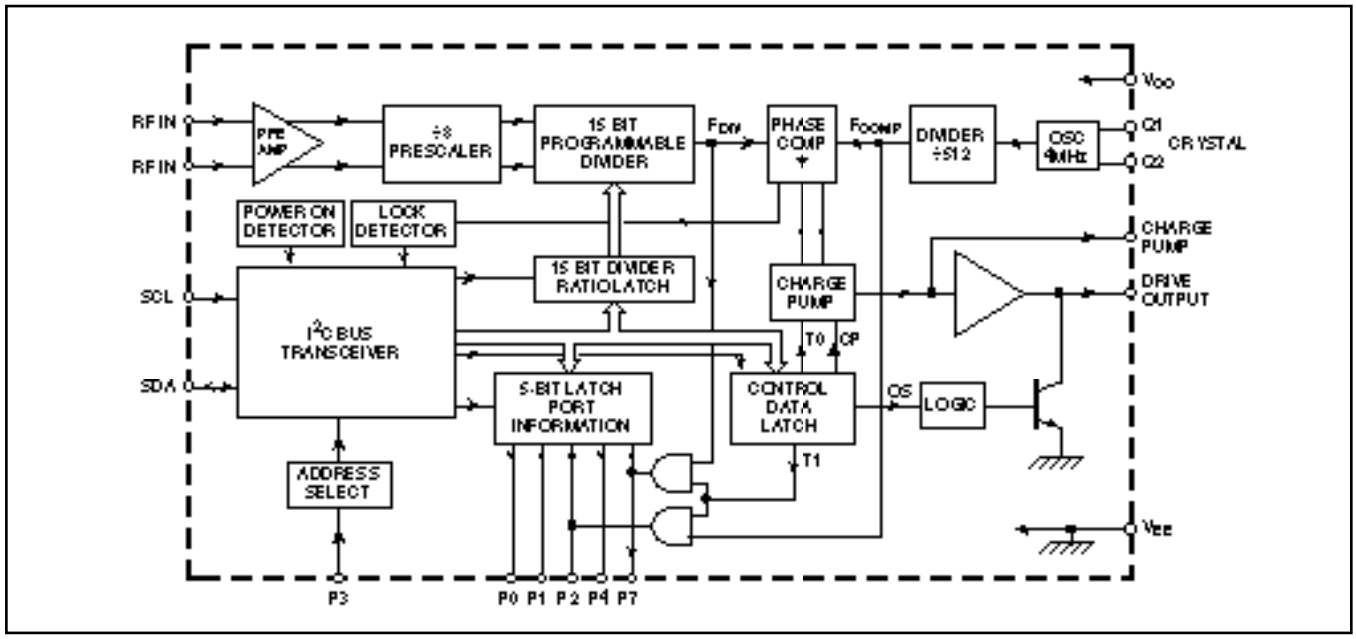


Fig. 2 Block diagram of SP5502S. (Ports P0 and P4 not present on SP5502F)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5502S (MP16 package).
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated. Reference frequency 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		48	60	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12·5		300	mVrms	80MHz to 1GHz
Prescaler input voltage		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	13,14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		V_{CC}	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500				V pin 16 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
Sink current	6,7,9-11	20			mA	V_{OUT} = 0·7V (see note 1)
Leakage current	6,7,9-11			10	µA	V_{OUT} = 13·2V
Input Port						
P3 input current high	8			1	mA	V pin 8 = V_{CC}
P3 input current low	8			−0·5	mA	V pin 8 = 0V

NOTES
1. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.
2. The maximum resistance quoted refers to all conditions, including start-up.

FUNCTIONAL DESCRIPTION (Except where otherwise indicated, 'SP5502' refers to both variants)

The SP5502 is programmed from an I^2C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C Bus system. Table 3 shows how the address is selected by applying a voltage to P3. The address input is shown in Fig. 6. The LSB of the address Byte (R/$\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5502 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5502 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P2 and P7, a logic 1 connects F_{COMP} to P2 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P2, P4 and P7 on the SP5502S (P1, P2 and P7 only on SP5502F), a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2. Bit 1 (POR) is the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	X	X	P4*	X	P2	P1	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	N	N	N	N	N	N	A	**Byte 2**

Table 2 Read data format

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}1V_{CC}$
0	1	Open circuit
1	0	$0{\cdot}4V_{CC}$ to $0{\cdot}6V_{CC}$†
1	1	$0{\cdot}9V_{CC}$ to V_{CC}

Table 3 Address selection

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 3)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P4*, P2, P1, P0*	:	Control output port states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
X	:	Don't care
N	:	Not valid

NOTES
† Programmed by connecting a 15kΩ resistor between Address Select Port P3 and V_{CC}.
* Don't care condition on SP5502F.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

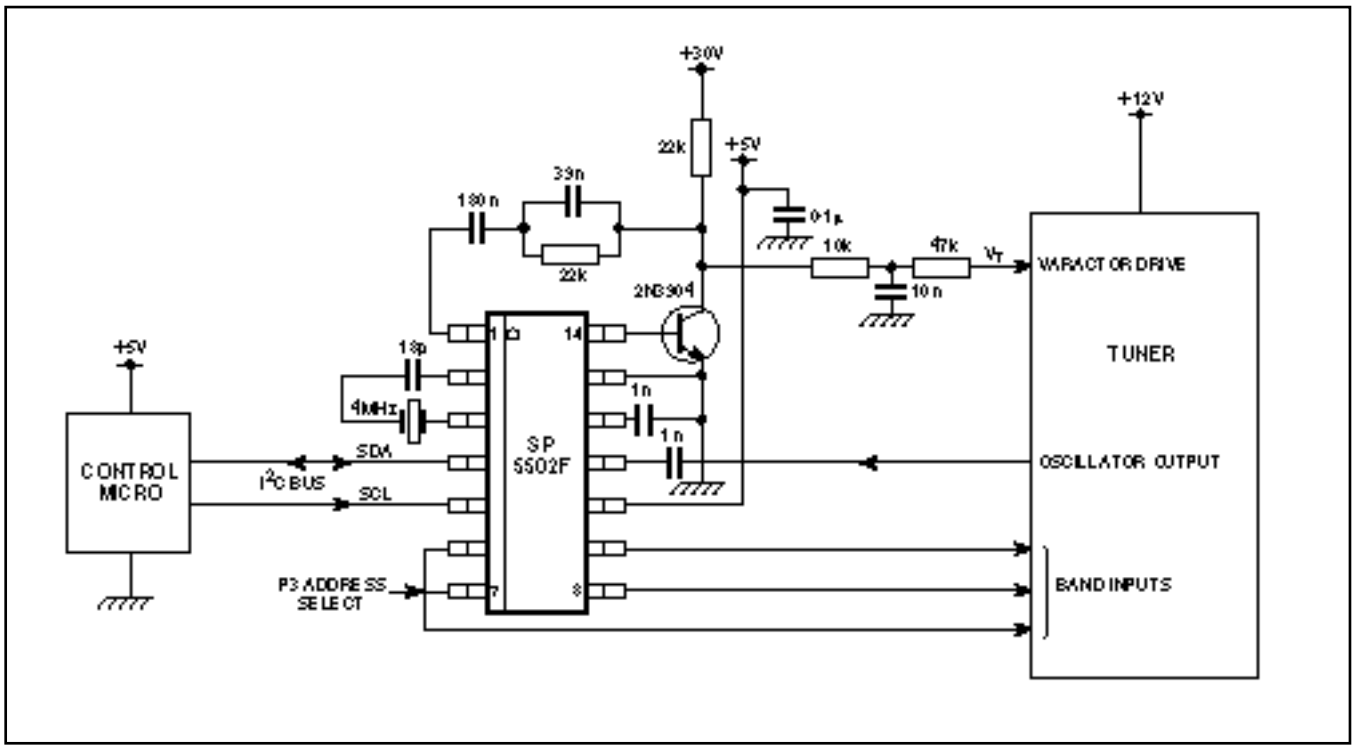


Fig. 4 Typical application

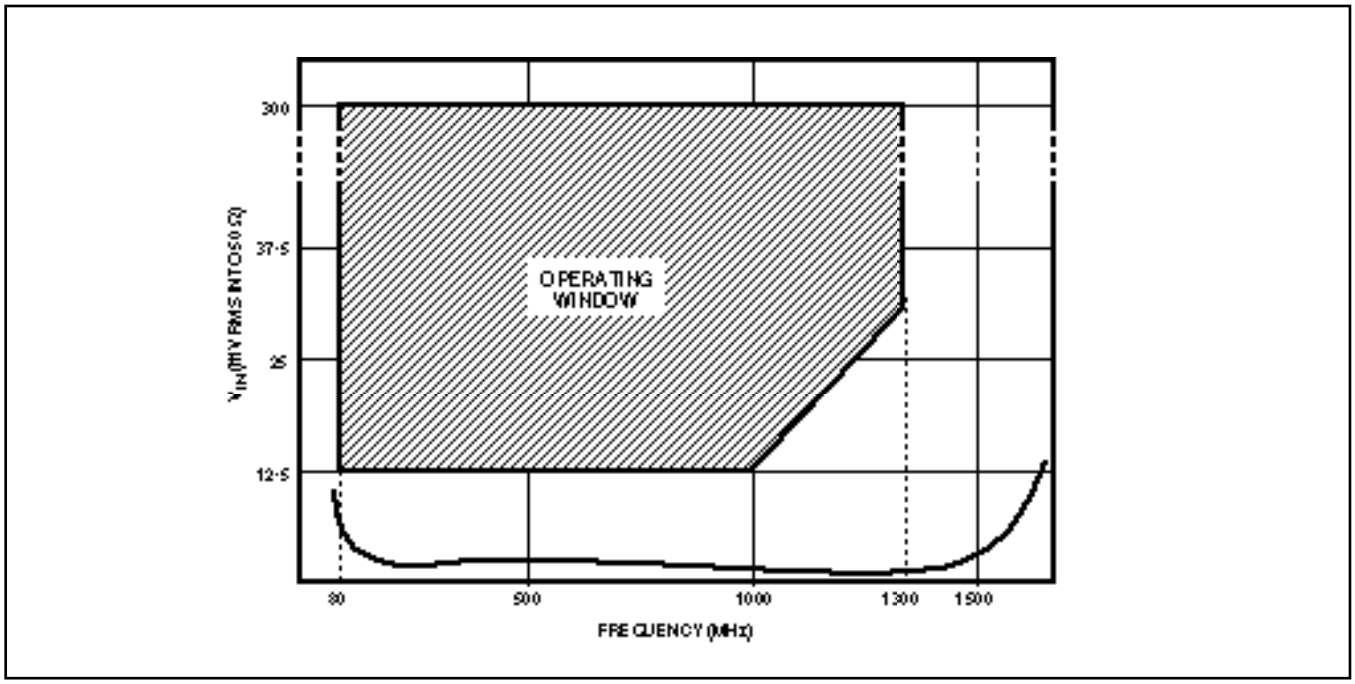


Fig. 5 Typical input sensitivity

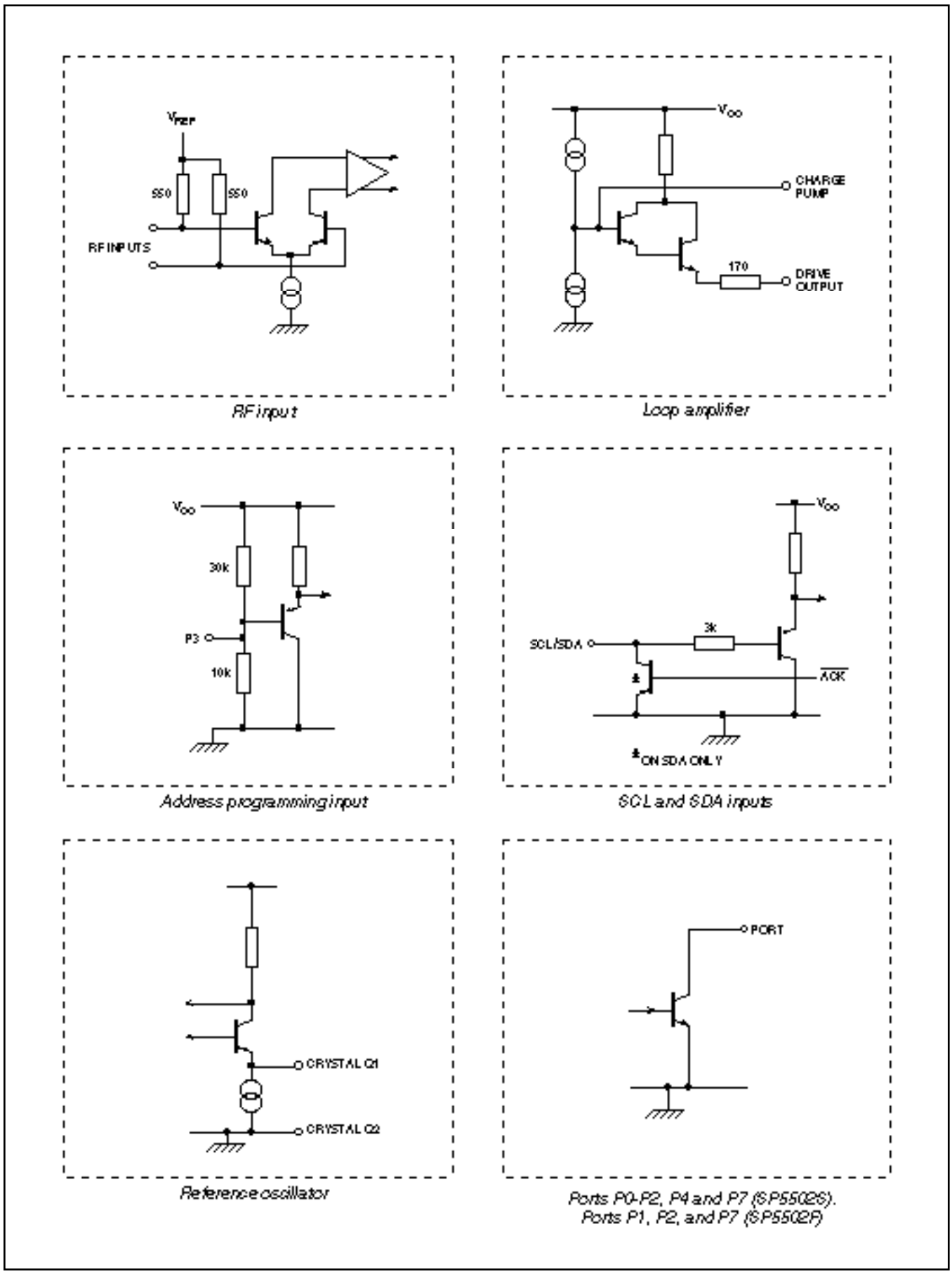


Fig. 6 SP5502 input/output interface circuits

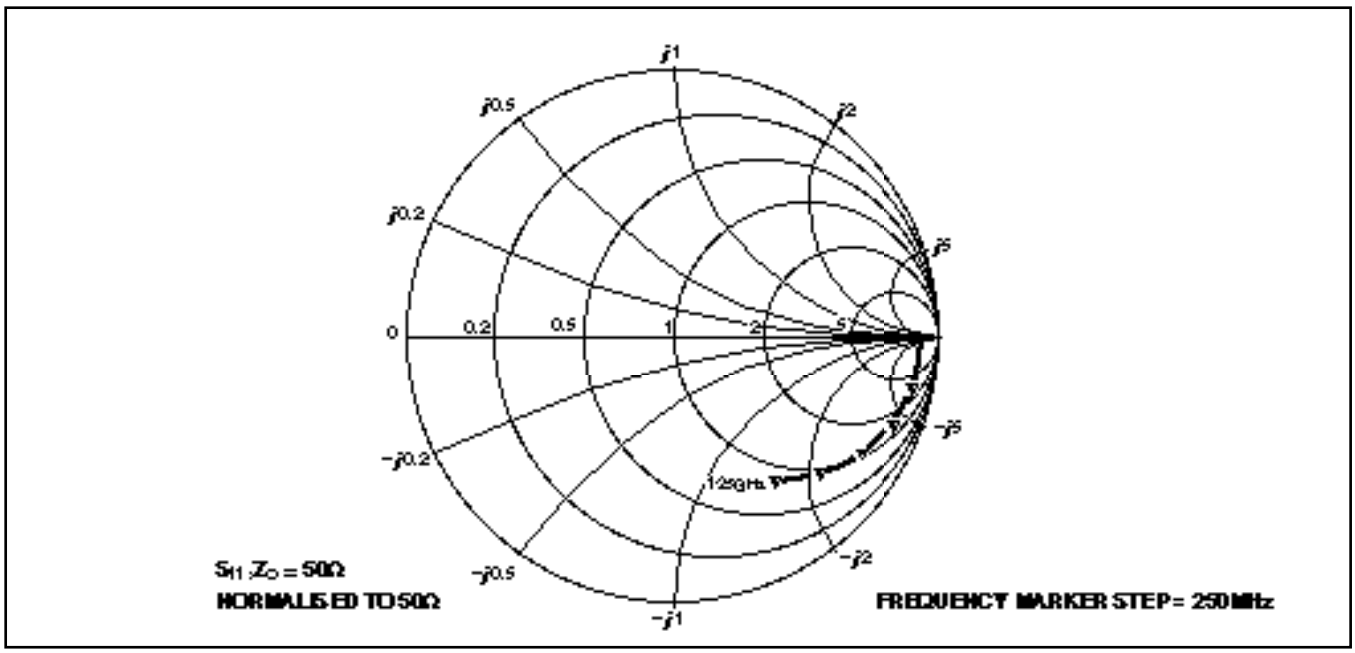


Fig. 7 Typical input impedance

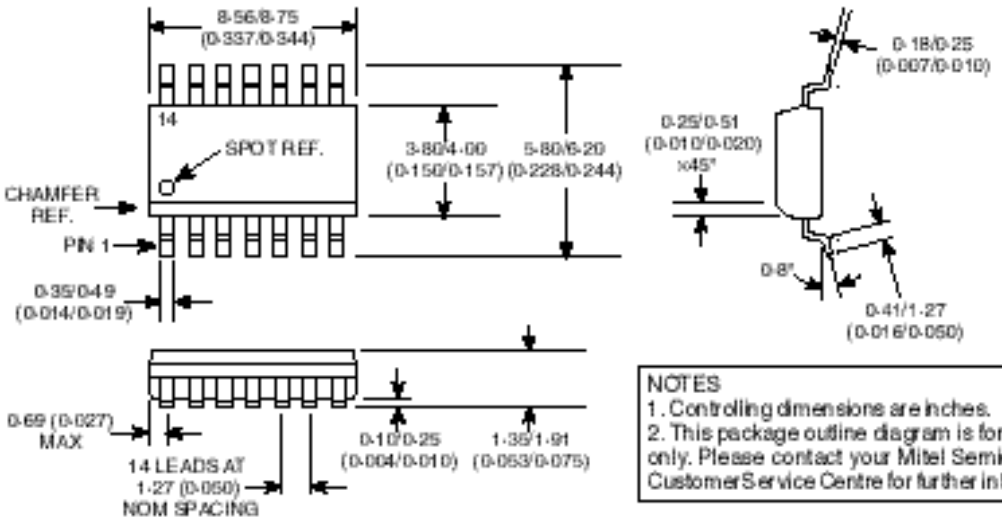
ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

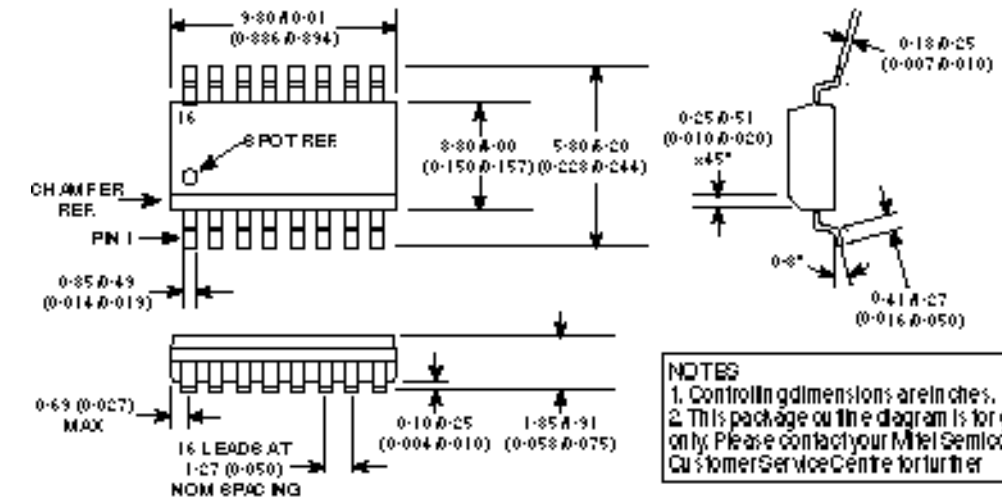
Parameter	Pin		Value		Units	Conditions
	SP5502S	SP5502F	Min.	Max.		
Supply voltage	12	10	−0·3	7	V	
RF input voltage	13,14	11,12		2·5	V p-p	
Port voltage	6,7, 9-11	6,8, 9	−0·3	14	V	Port in off state
	6,7, 9-11	6,8, 9	−0·3	6	V	Port in on state
	8	7	−0·3	V_{CC}+0·3	V	
Total port output current	6,7, 9-11	6,8, 9		50	mA	
RF input DC offset	13,14	11,12	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	16	14	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
			−0·3	5·5	V	V_{CC} not applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
MP14 thermal resistance, chip-to-ambient				123	°C/W	
MP14 thermal resistance, chip-to-case				45	°C/W	
Power consumption at 5·5V				363	mW	

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



14-LEAD MINIATURE PLASTIC DIL - MP14



16-LEAD MINIATURE PLASTIC DIL - MP16

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